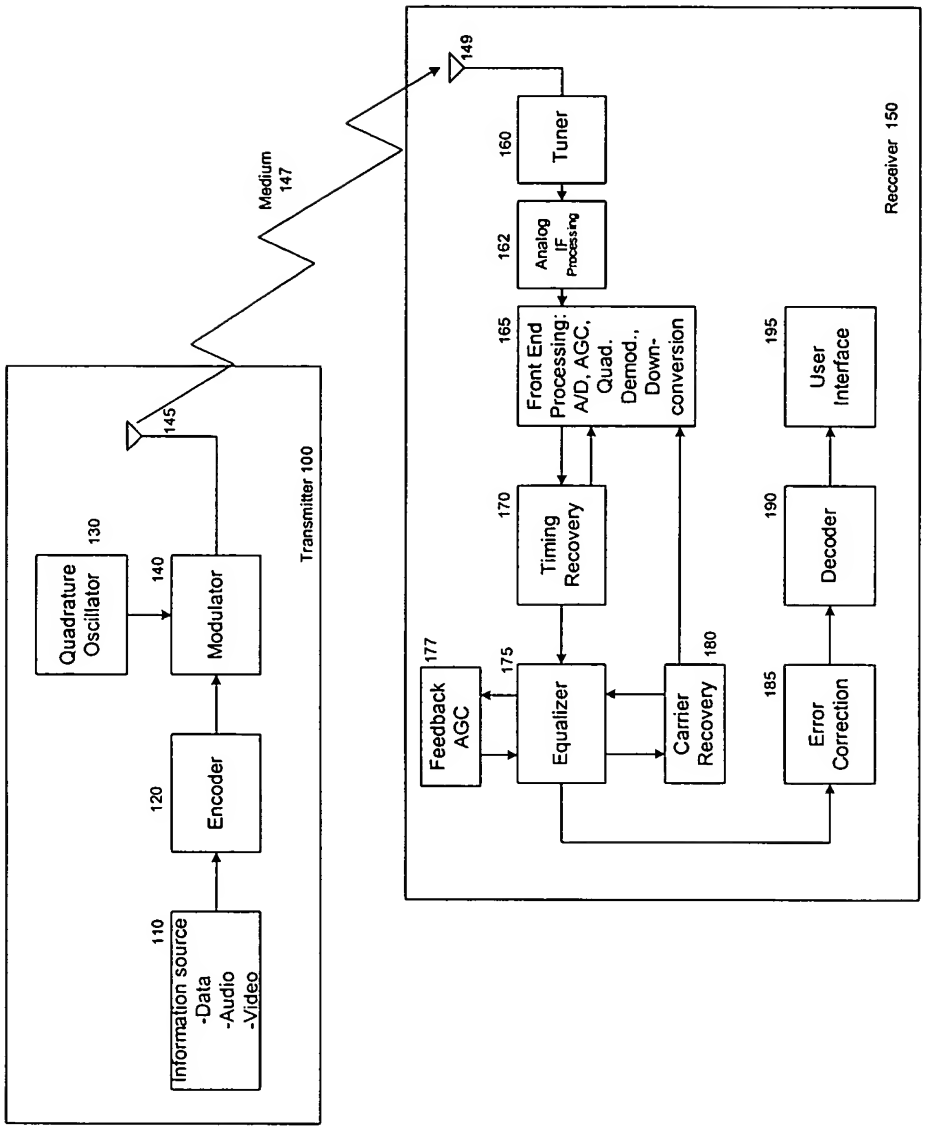

Figure 1: Typical prior-art communication system that may be employed for transmission of digital signals.

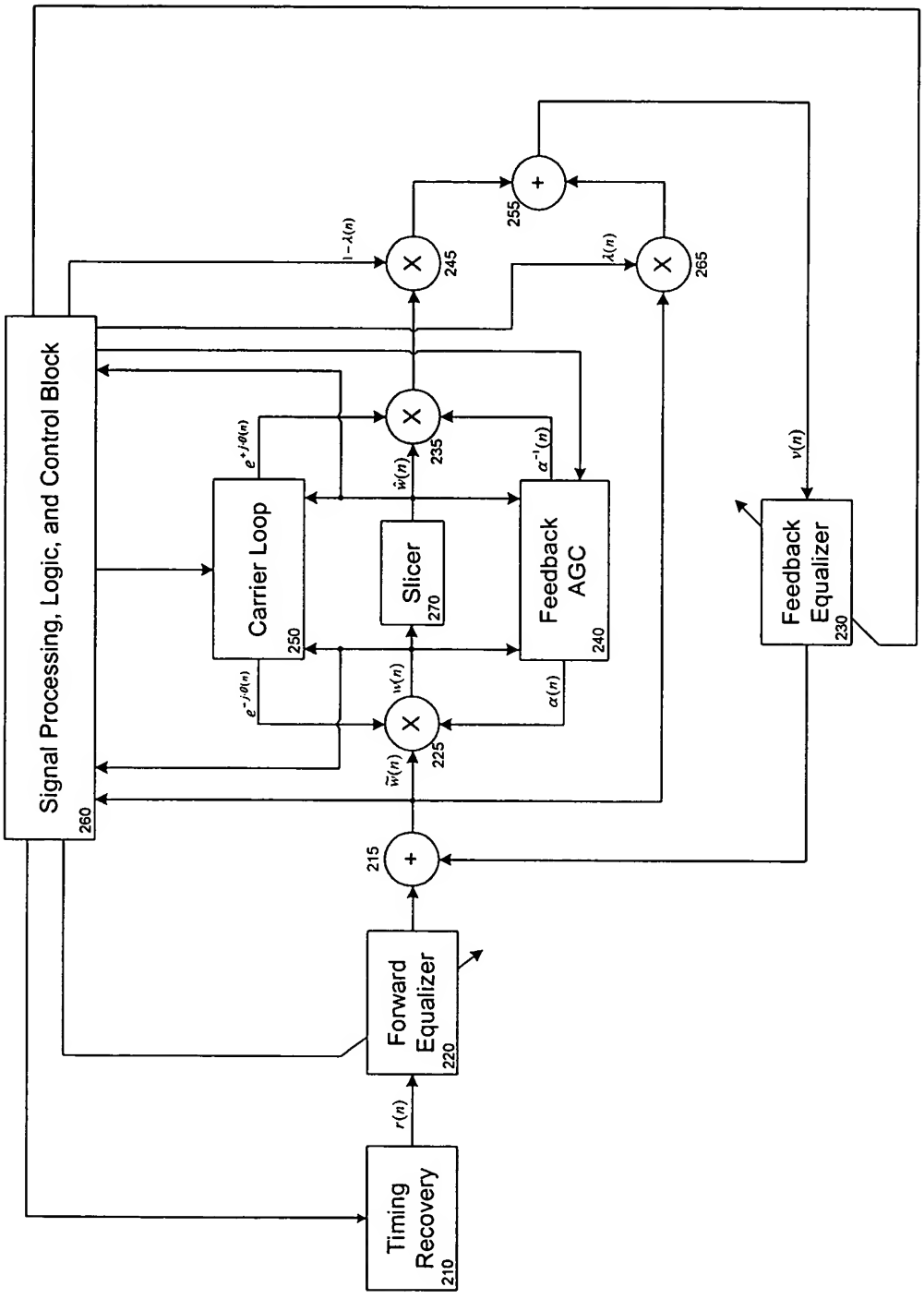

Figure 2: Block diagram of timing recovery, equalization, carrier recovery, and automatic gain control, jointly controlled by a central signal processing block in accordance with the present invention.

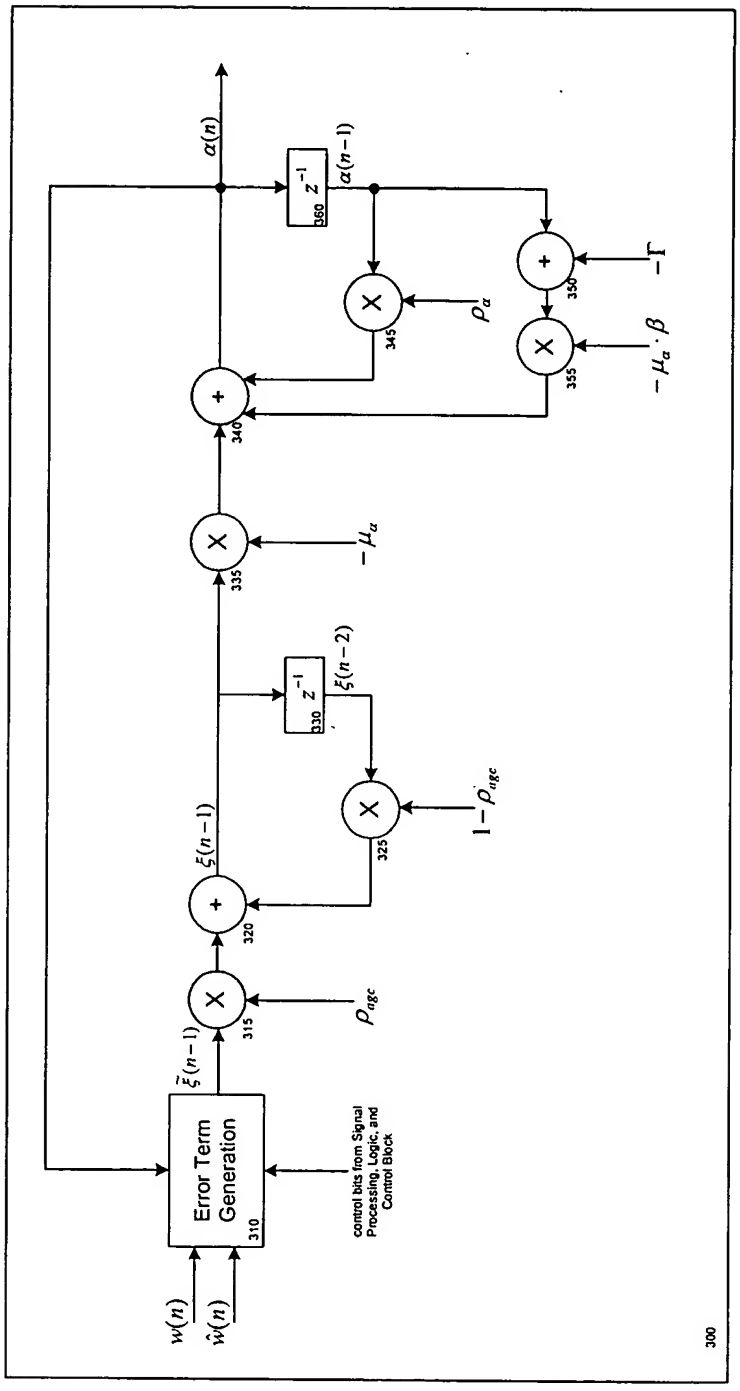

Figure 3: Diagram of preferred embodiment of Feedback AGC, showing adaptation of gain value at each symbol instance, and error term selection using control signals in accordance with the present invention.

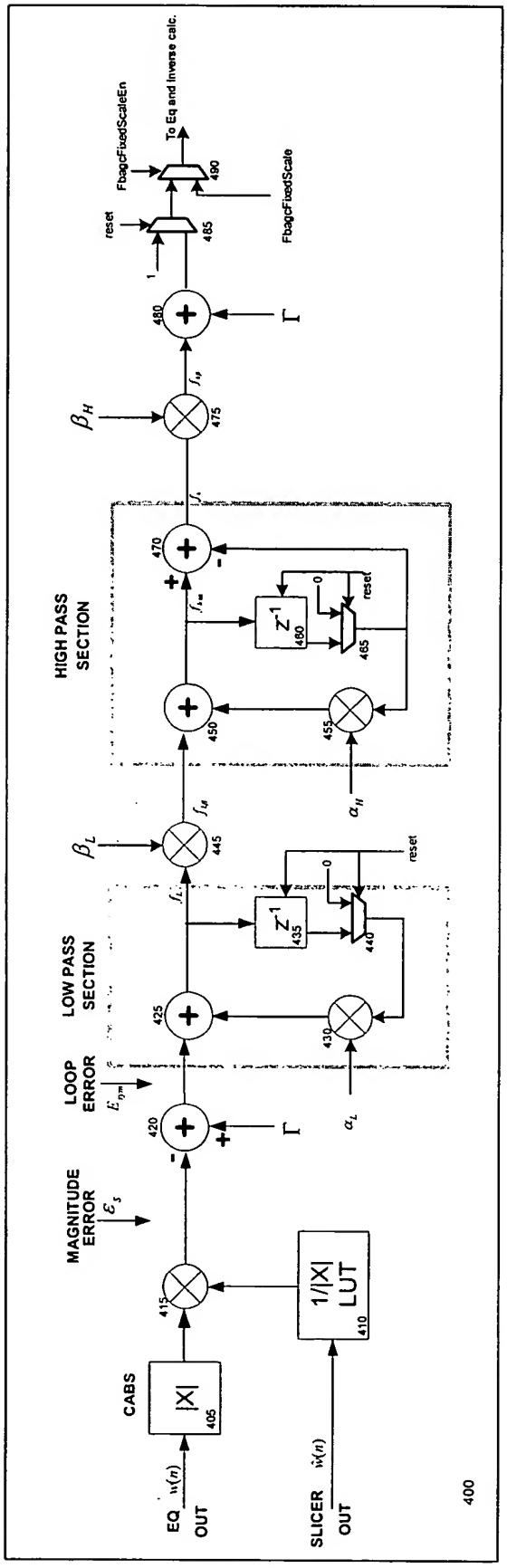

Figure 4: Diagram of alternative embodiment of Feedback AGC, showing error term generation, and bandpass filtering using cascaded low-pass and high-pass filter sections, in accordance with the present invention.

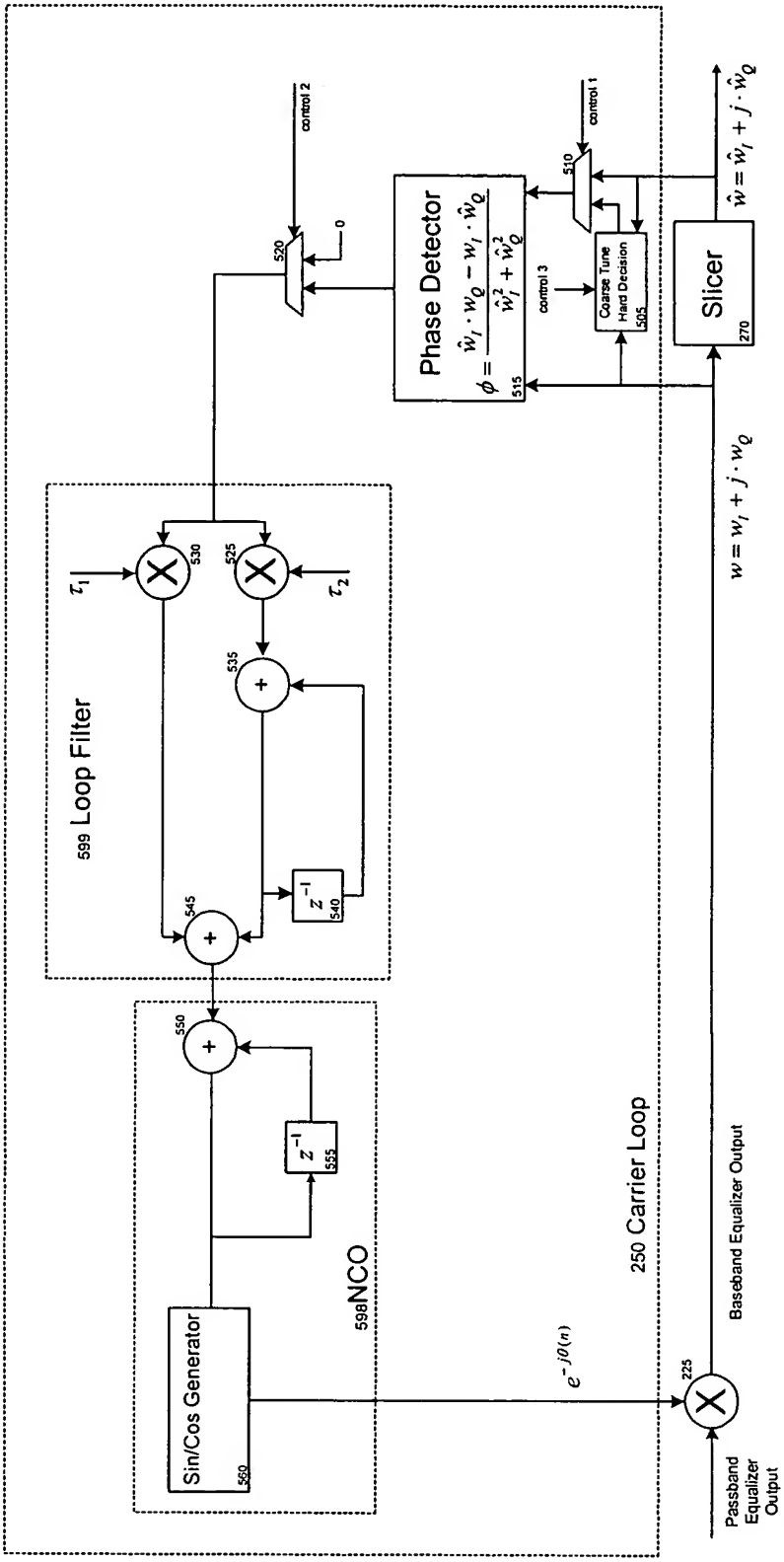

Figure 5: Diagram of Carrier Loop nested with Equalizer and Slicer, used to translate the received signal to precise baseband.

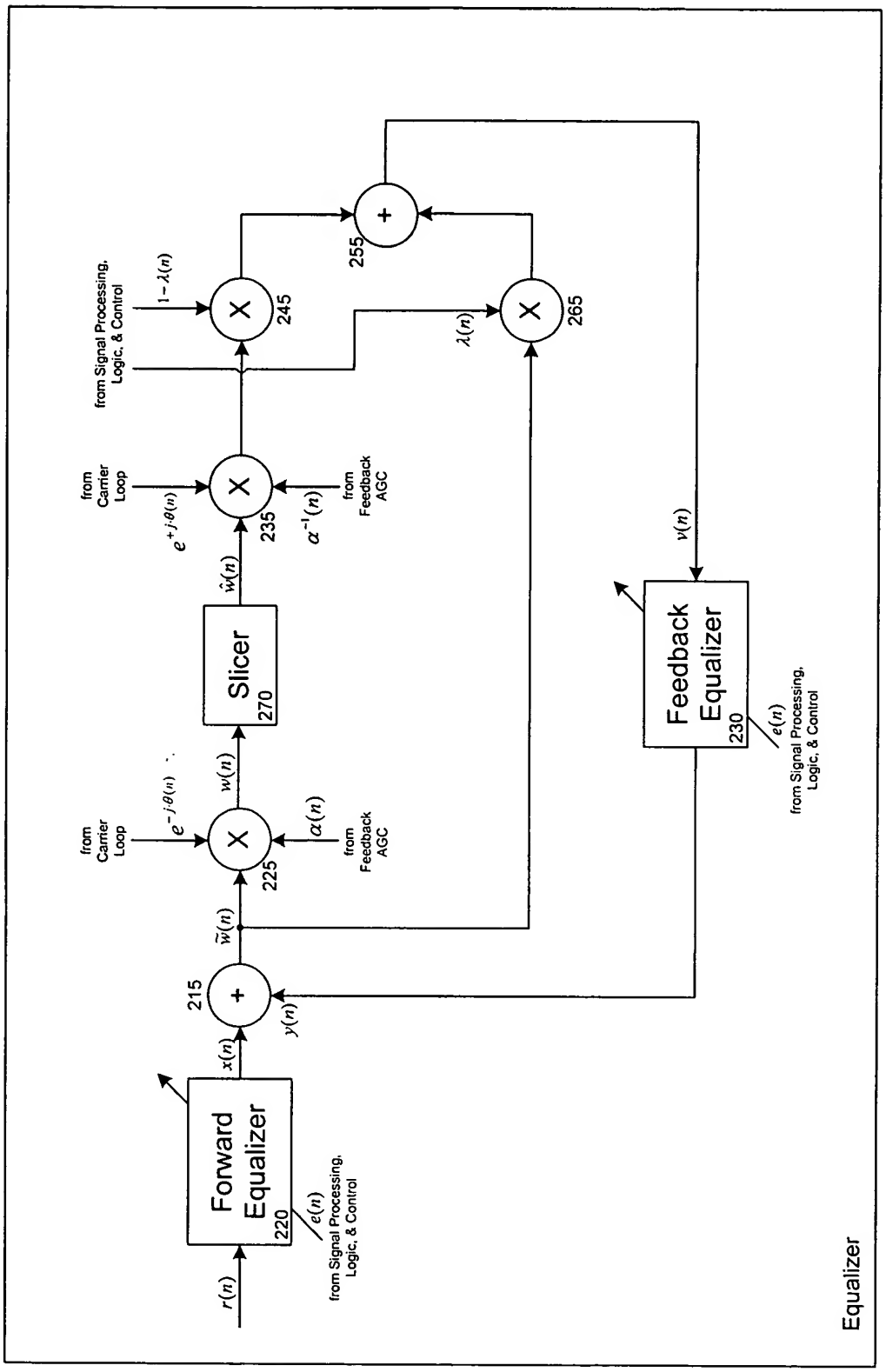

Figure 6: Block diagram of Decision Feedback Equalizer (DFE) in accordance with the present invention.

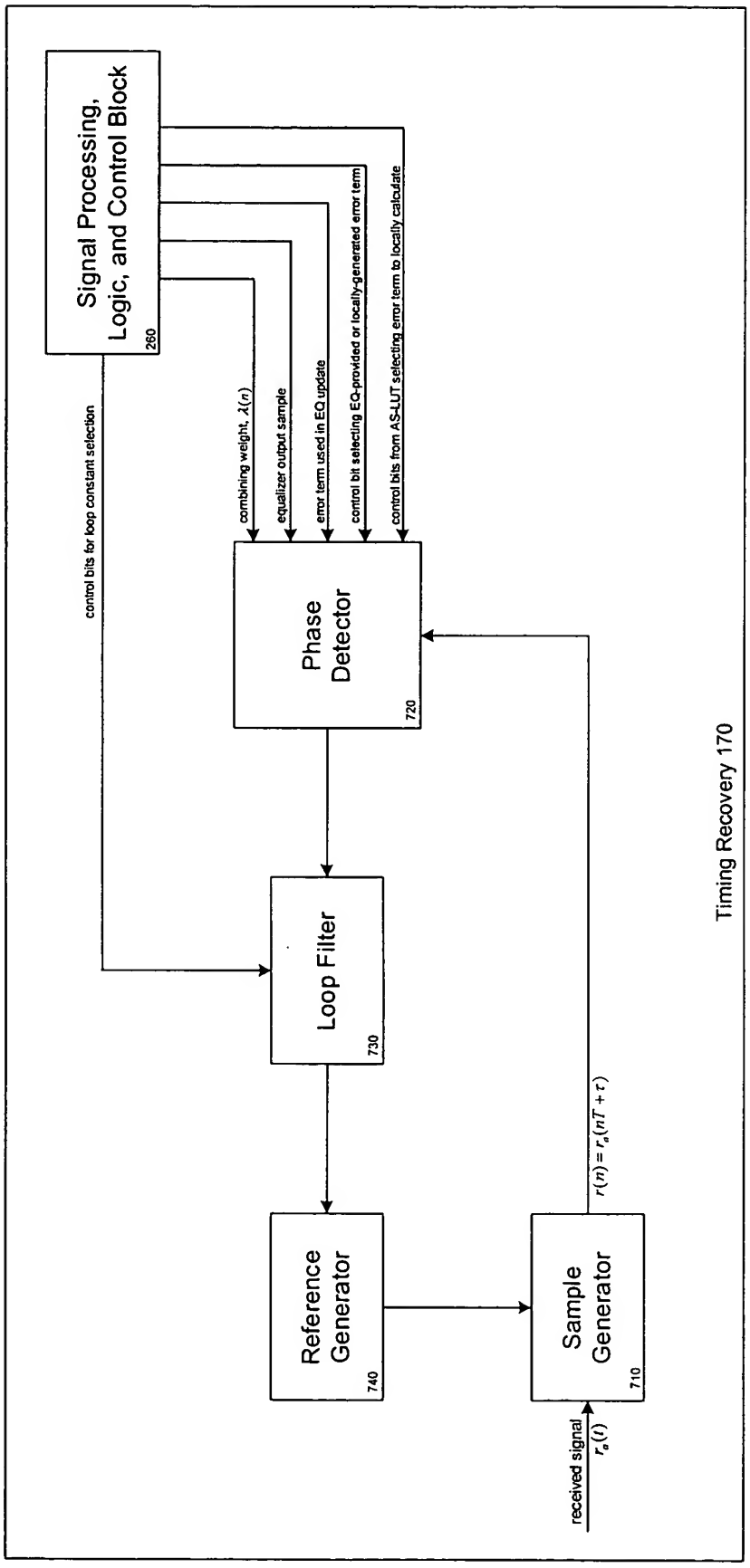

Figure 7: Block diagram of Timing Recovery Loop 170 and its control by Signal Processing, Logic, and Control Block 260 in accordance with the present invention.

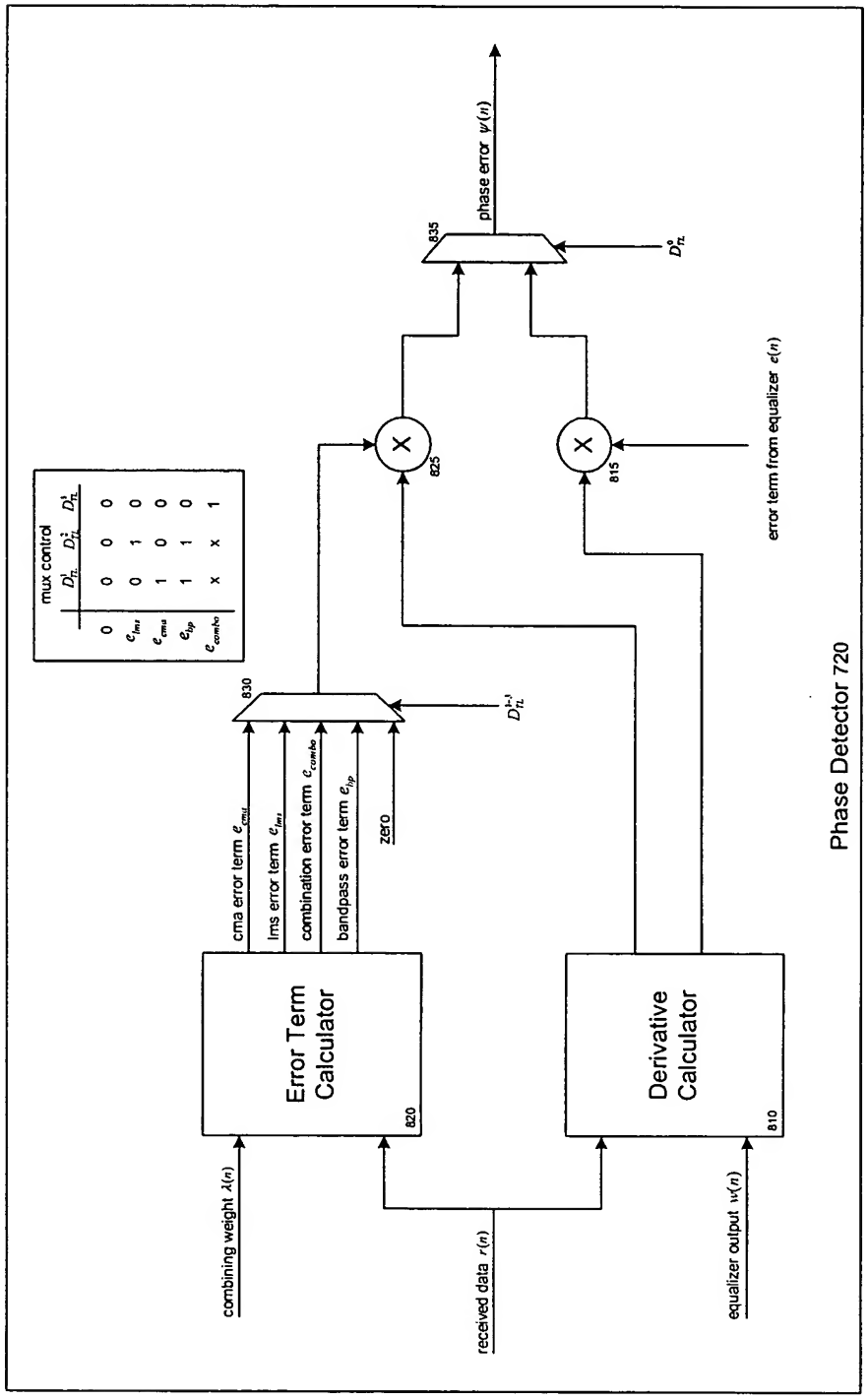

Figure 8: Phase Detector for Timing Recovery Loop and its control by the Signal Processing, Logic, and Control Block

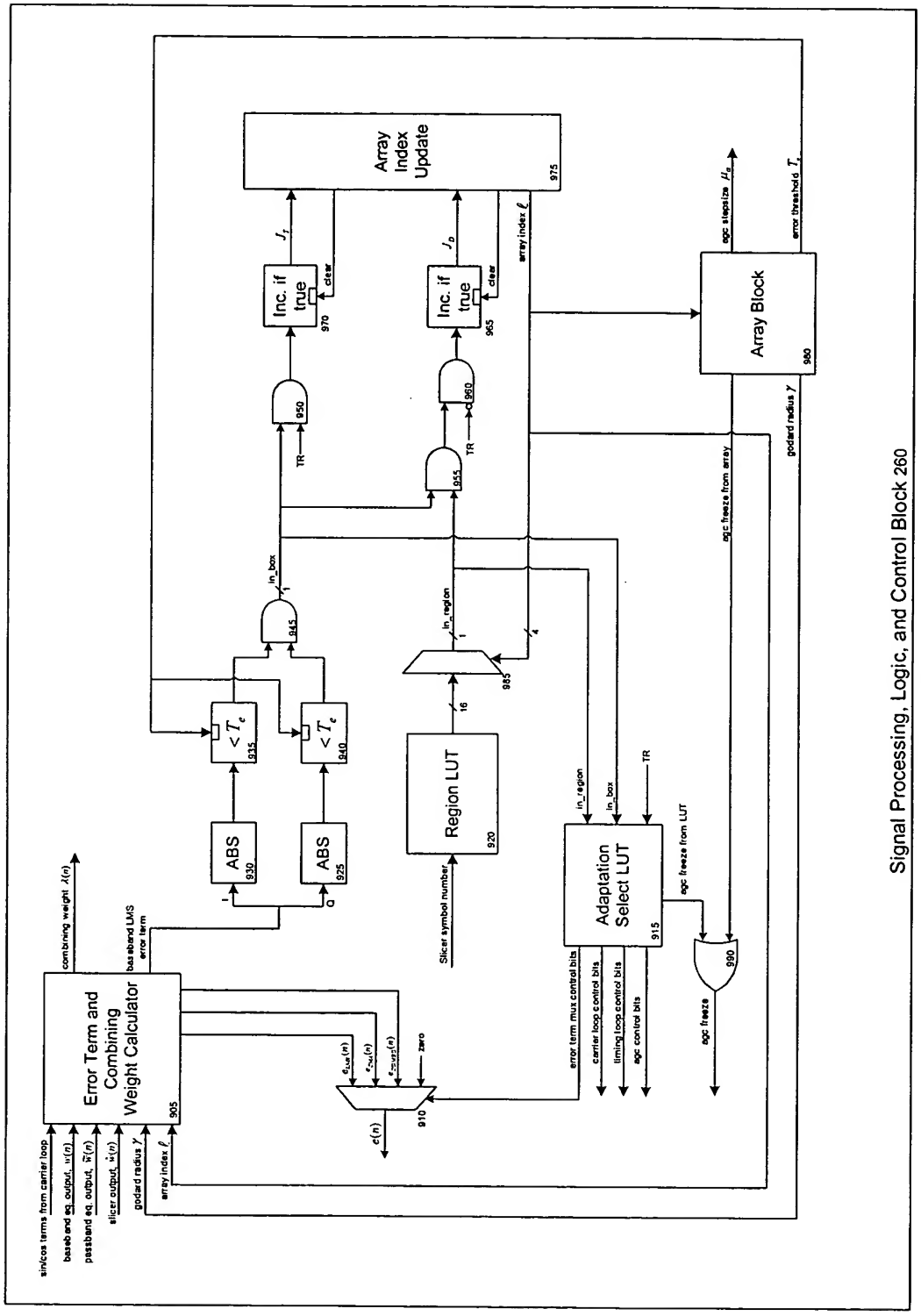

Figure 9: Signal Processing, Logic, and Control Block

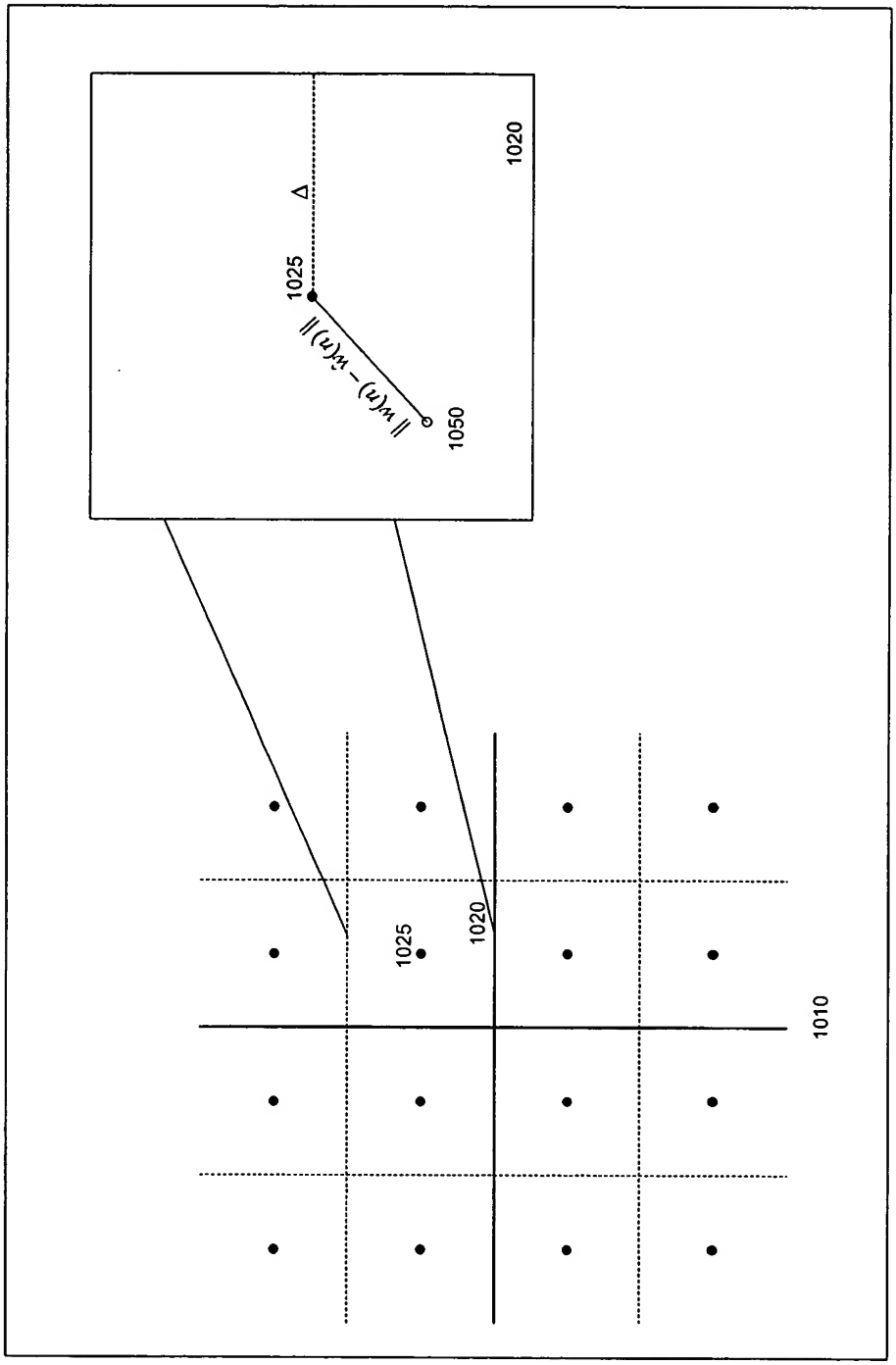

Figure 10: Conceptual illustration of combining weight calculation.

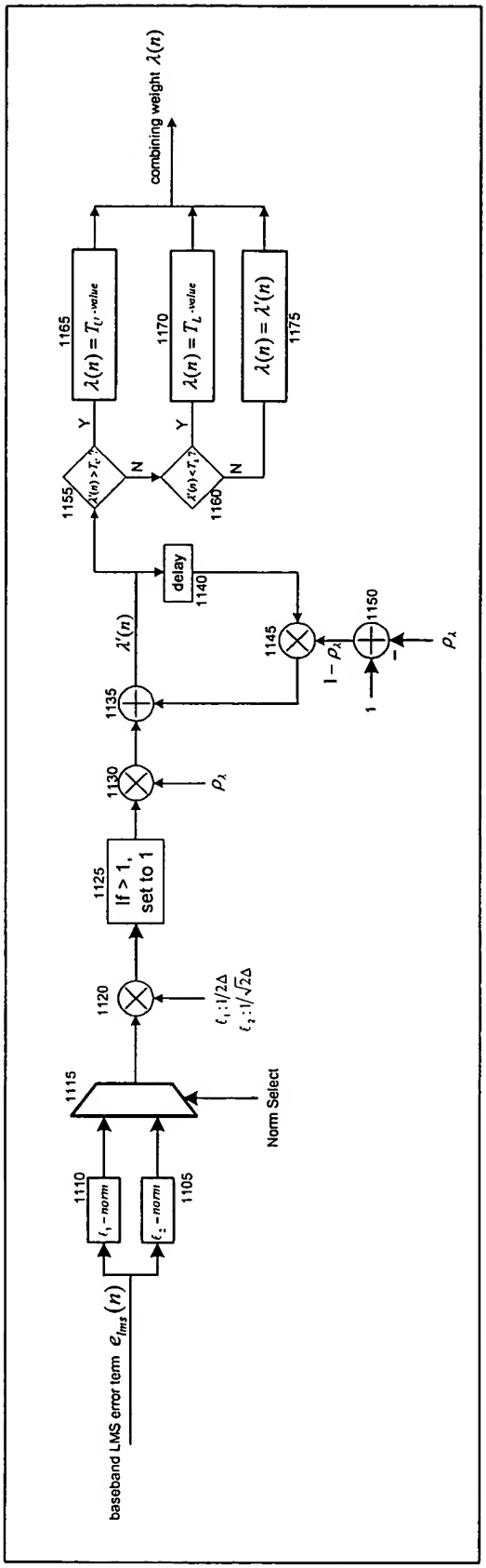

Figure 11: Circuit used to calculate combining weight $\lambda(n)$ in accordance with the present invention.

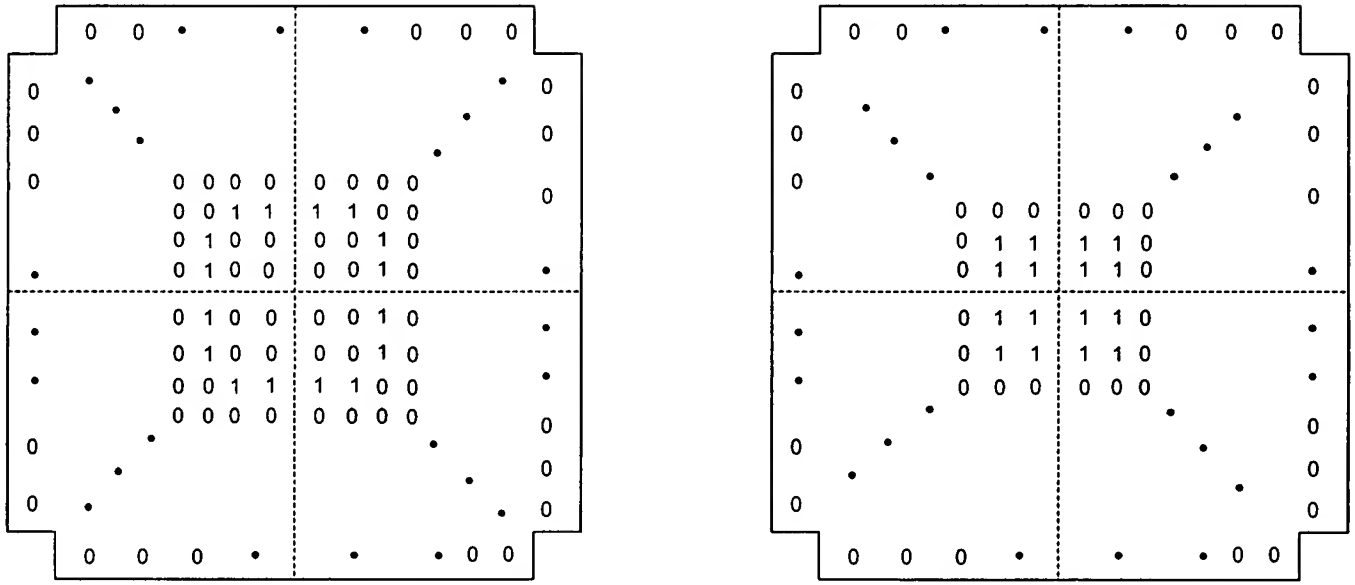

Figure 12: Conceptual drawing illustrating two possible templates used to discern a control signal in accordance with the present invention.

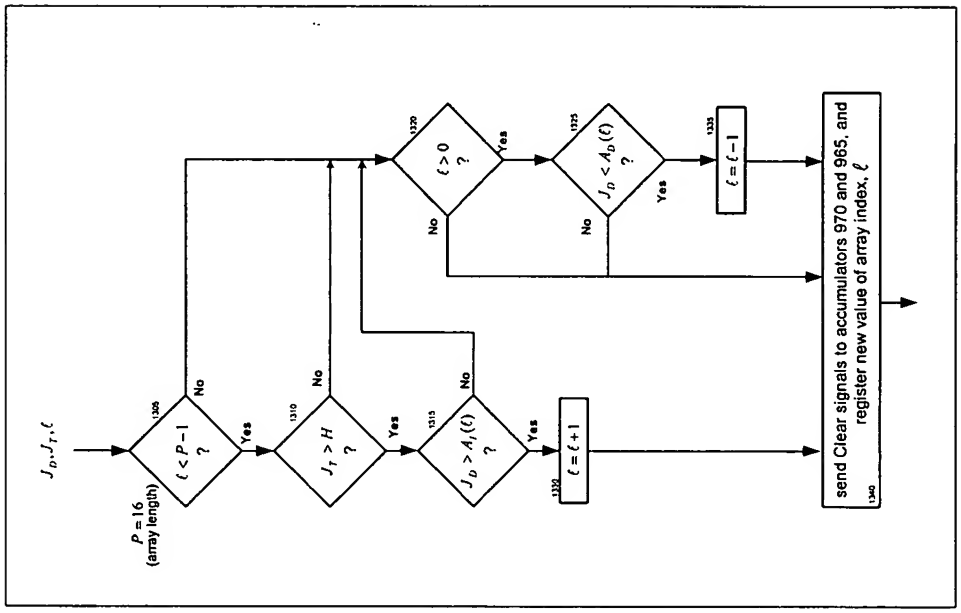

Figure 13:Flow diagram illustrating the update of array index ℓ in accordance with the present invention.